REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The office action dated January 26, 2004 has been received and its contents carefully reviewed.

Claims 1-25 remain in the application. Claims 1, 9, 17, and 19 are amended. Applicant wishes to thank the Examiner for the indication that claims 2-8, 10-16, 18, and 20-25 contain allowable subject matter.

In the Office Action, claims 1, 9, 17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Related Art ("ARA") in view of U.S. Patent No. 5,285,301 to Shirahashi et al ("Shirahashi").

The rejection of claims 1, 9, 17, and 19 under 35 U.S.C. § 103(a) as being unpatentable over ARA in view of Shirahashi is respectfully traversed and reconsideration is requested. Claim 1 is allowable over the cited reference in that claim 1 recites a combination of elements including, for example "a dummy data line included in a non-display area outside the display area and formed in parallel to the data lines, to allow each pixel to have substantially a same parasitic capacitance." Claim 9 is allowable over the cited reference in that claim 9 recites a combination of elements including, for example "a dummy data line for compensating a capacitor value difference of an adjacent pixel electrode thereto to allow each pixel to have substantially a same parasitic capacitance." Claim 17 is allowable over the cited reference in that claim 17 recites a combination of elements including, for example "supplying a signal to the dummy data line in a non-display area to allow each pixel to have a substantially same parasitic capacitance." Claim 19 is allowable over the cited reference in that claim 19 recites a combination of elements including, for example "a dummy data line formed in parallel to the data lines to allow each pixel to have substantially a same parasitic capacitance." The ARA and Shirahashi, singly or in combination, do not teach or suggest at least these features of the claimed invention.

Shirahashi discloses dummy lines DDL disposed outside the outermost signal data line DL to reduce the likelihood of the outmost signal line DL from breaking. The Examiner

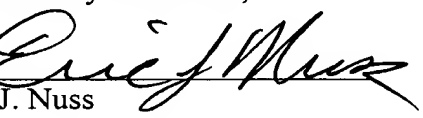
states that "Shirahashi et al is cited to teach a liquid crystal display device having peripheral dummy lines which can compensate a capacitor value difference of an adjacent pixel electrode since each pixel includes a capacitor Cadd as claimed (see fig. 15, Cadd)." In Shirahashi Cadd includes the pixel electrode and the gate line. This is different from the present invention, where the parasitic capacitance results from capacitance between the pixel electrode and an adjacent pixel's data line. Accordingly, Applicants respectfully submit that claims 1, 9, 17, and 19 are allowable over the cited references.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: April 26, 2004

Respectfully submitted,

By 

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